Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
L20	l5 and l19	0	L20
L19	memory near3 (partition$4 or allocat$3) same (clear data or color pixel)	33	L19
L18	L16 and color near3 pixel	0	L18
L17	L16 and clear near3 data	0	L17
L16	L15 and controller	12	L16
L15	l10 and memory	14	L15
L14	l10 and (sub-region or sub-section or sub-unit or sub-cell or sub-block or subregion or subsection or subcell or subunit or subblock)	0	L14
L13	l10 and (sub-region or sub-section or sub-unit or sub-cell or sub-block or subregion or subsection or subcell or subunit or subblock)	0	L13
L12	l10 and (sub-region or sub-section or sub-unit or sub-cell or sub-block or subregion or subsection or subcell or subunit or subblock) same controller	0	L12
L11	l9 and (sub-region or sub-section or sub-unit or sub-cell or sub-block or subregion or subsection or subcell or subunit or subblock) same controller	1	L11
L10	(4545014| 4847750| 5005121| 5291582| 5404522| 5440687| 5724583| 5724587)![pn]	14	L10
L9	6219725.pn.	2	L9
L8	L5 and (clear data or color pixel)	16	L8
L7	L5 same (clear near2 data or color near2 pixel)	0	L7
L6	L5 same (clear data or color pixel)	0	L6
L5	L4 not l2	206	L5
L4	memory near5 (sub-region or sub-section or sub-unit or sub-cell or sub-block or subregion or subsection or subcell or subunit or subblock) same controller	220	L4
L3	L2 not l1	3	L3
L2	memory near3 (plurality or multiple or more than one or various or numerous) near3 (sub-region or sub-section or sub-unit or sub-cell or sub-block or subregion or subsection or subcell or subunit or subblock) same controller	14	L2
L1	memory adj3 (plurality or multiple or more than one or various or numerous) near2 (sub-region or sub-section or sub-unit or sub-cell or sub-block or subregion or subsection or subcell or subunit or subblock) same controller	11	L1

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 11 of 11 returned.

1. Document ID: US 20030177300 A1

L27: Entry 1 of 11 File: PGPB Sep 18, 2003

DOCUMENT-IDENTIFIER: US 20030177300 A1
TITLE: Data processing method in high-capacity flash EEPROM card system

Summary of Invention Paragraph (20):
[0018] Another aspect of the present invention provides a data processing method in a high-capacity flash EEPROM card system mounted with at least one flash EEPROM and a controller connected to a host computer, having an interface for down/up loading arbitrary data into the flash EEPROM data regions to access the host computer, in which a data writing operation method in the flash EEPROM system for setting a designated number of block regions that divide the flash EEPROM data regions into a designated arbitrary size and for sub-dividing each block region to a designated number of mapping table regions includes: a first procedure for transmitting CHS (Cylinder, Head, and Sector)value to let the host access data files in the flash EEPROM; a second procedure for generating logical block address (LBA) on the basis of the transmitted CHS from the first procedure and for deciding whether or not the generated LBA's range exceeds full capacity of the flash EEPROM; a third procedure for storing the data transmitted from the host in volatile memory inside of the controller and for converting the stored data to physical block address (PBA); a fourth procedure for obtaining an index number of the mapping table region based on the PBA and for comparing the index number with a previous index number; a fifth procedure for storing a current look-up-table in the flash EEPROM, if the new index number obtained in the fourth procedure is not identical with the previous index number, loading a look-up-table corresponding to the new index number from the flash EEPROM, and for changing the new index number back to the previous index number; and a sixth procedure for obtaining a new PBA for use of the flash EEPROM from "Queue" block table of the volatile EEPROM inside of the controller, writing data from a data buffer inside of the volatile EEPROM on a corresponding mapping table region of a relevant flash EEPROM on the basis of the new PBA, and for updating the look-up-table.

Summary of Invention Paragraph (21):
[0019] Still another aspect of the present invention provides a data processing method in a high-capacity flash EEPROM card system mounted with at least one flash EEPROM and a controller connected to a host computer, having an interface for down/up loading arbitrary data into the flash EEPROM data regions to access the host computer, in which a data reading operation method in the flash EEPROM system for setting a designated number of block regions that divide the flash EEPROM data regions into a designated arbitrary size and for sub-dividing each block region to a designated number of mapping table regions includes: a first procedure for transmitting CHS (Cylinder, Head, Sector)value to let the host access data files in the flash EEPROM; a second procedure for generating logical block address (LBA) on the basis of the transmitted CHS from the first procedure and for deciding whether or not the generated LBA's range exceeds full capacity of the flash EEPROM; a third procedure for storing the data transmitted from the host in volatile memory inside of the controller and for converting the stored data to physical block address (PBA); a fourth procedure for obtaining an index number of the mapping table region based on the PBA and for comparing the index number with a previous index number; a fifth procedure for storing a current look-up-table in the flash EEPROM, if the new index number obtained in the fourth procedure is not identical with the previous index number, loading a look-up-table corresponding to the new index number from the flash EEPROM, and for changing the new index number back to the previous index number; and a sixth procedure for transmitting data corresponding to the loaded look-up-table in the fifth procedure to the host side.

CLAIMS:

2. A data writing method in a high-capacity flash erasable and programmable read-only memory (EEPROM) card system mounted with at least one flash EEPROM and a controller connected to a host computer, having an interface for down/up loading arbitrary data into the flash EEPROM data regions to access the host computer,

wherein the data writing operation method in the flash EEPROM system for setting a designated number of block regions that divide the flash EEPROM data regions into a designated arbitrary size and for sub-dividing each block region to a designated number of mapping table regions comprises: a first procedure for transmitting CHS (Cylinder, Head, and Sector)value to let the host access data files in the flash EEPROM; a second procedure for generating logical block address (LBA) on the basis of the transmitted CHS from the first procedure and for deciding whether or not the generated LBA's range exceeds full capacity of the flash EEPROM; a third procedure for storing the data transmitted from the host in volatile memory inside of the controller and for converting the stored data to physical block address (PBA); a fourth procedure for obtaining an index number of the mapping table region based on the PBA and for comparing the index number with a previous index number; a fifth procedure for storing a current look-up-table in the flash EEPROM, if the new index number obtained in the fourth procedure is not identical with the previous index number, loading a look-up-table corresponding to the new index number from the flash EEPROM, and for changing the new index number back to the previous index number; and a sixth procedure for obtaining a new PBA for use of the flash EEPROM from "Queue" block table of the volatile memory inside of the controller, writing data from a data buffer inside of the volatile memory on a corresponding mapping table region of a relevant flash EEPROM on the basis of the new PBA, and for updating the look-up-table.

3. A data reading method in a high-capacity flash erasable and programmable read-only memory (EEPROM) card system mounted with at least one flash EEPROM and a controller connected to a host computer, having an interface for down/up loading arbitrary data into the flash EEPROM data regions to access the host computer, wherein the data reading method in the flash EEPROM system for setting a designated number of block regions that divide the flash EEPROM data regions into a designated arbitrary size and for sub-dividing each block region to a designated number of mapping table region comprises: a first procedure for transmitting CHS (Cylinder, Head, and Sector) value to let the host access data files in the flash EEPROM; a second procedure for generating logical block address (LBA) on the basis of the transmitted CHS from the first procedure and for deciding whether or not the generated LBA's range exceeds full capacity of the flash EEPROM; a third procedure for storing the data transmitted from the host in volatile memory inside of the controller and for converting the stored data to physical block address (PBA); a fourth procedure for obtaining an index number of the mapping table region based on the PBA and for comparing the index number with a previous index number; a fifth procedure for storing a current look-up-table in the flash EEPROM, if the new index number obtained in the fourth procedure is not identical with the previous index number, loading a look-up-table corresponding to the new index number from the flash EEPROM, and for changing the new index number back to the previous index number; and a sixth procedure for transmitting data corresponding to the loaded look-up-table in the fifth procedure to the host side.

☐ 2. Document ID: US 20030093644 A1

L27: Entry 2 of 11 File: PGPB May 15, 2003

DOCUMENT-IDENTIFIER: US 20030093644 A1
TITLE: CACHE LINE REPLACEMENT POLICY ENHANCEMENT TO AVOID MEMORY PAGE THRASHING

Detail Description Paragraph (18):
[0030] In a chipset memory controller, memory is typically divided into a number of banks. The particular number of memory banks deployed in any platform depends on factors such as the DRAM technology used and the number of devices populating the system. With a single dual in-line memory module (DIMM) of synchronous DRAM (SDRAM) for example, a computer system can have as few as four banks. In a fully populated Rambus DRAM (RDRAM) memory subsystem, the chipset can control about a thousand banks. The size of a bank is equal to the size of the memory system divided by the number of banks in the memory system. These banks are further subdivided into a number of pages that can range in size from 1 kilobyte (Kbyte) to 64 Kbyte.

☐ 3. Document ID: US 20010016784 A1

L27: Entry 3 of 11 File: PGPB Aug 23, 2001

DOCUMENT-IDENTIFIER: US 20010016784 A1
TITLE: Audio data storage device

Summary of Invention Paragraph (11):
[0010] To solve this problem, a method using a single memory has been proposed (in Japanese Unexamined Patent Application, First Publication No. Hei 10-271082). This method divides the buffer memory for storing the PCM data into a plurality of regions. Further, a register for storing values which indicates whether the PCM data can be written into the divided regions, and a storage section for storing time information for outputting the PCM data from the regions, are provided. A controller outputs the PCM data from the buffer memory based on the time information stored in the storage section. Whenever the PCM data is output from the buffer memory, the controller records in the register that the region from which the PCM data has been output is writable. When the PCM data is input from an external device, the data is stored into the storage region in the buffer memory based on the information stored in the register. This method requires the subdivision and management of the buffer memory to reduce the size of the buffer memory.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 4. Document ID: US 6625695 B2

L27: Entry 4 of 11 File: USPT Sep 23, 2003

DOCUMENT-IDENTIFIER: US 6625695 B2
TITLE: Cache line replacement policy enhancement to avoid memory page thrashing

Detailed Description Text (18):
In a chipset memory controller, memory is typically divided into a number of banks. The particular number of memory banks deployed in any platform depends on factors such as the DRAM technology used and the number of devices populating the system. With a single dual in-line memory module (DIMM) of synchronous DRAM (SDRAM) for example, a computer system can have as few as four banks. In a fully populated Rambus DRAM (RDRAM) memory subsystem, the chipset can control about a thousand banks. The size of a bank is equal to the size of the memory system divided by the number of banks in the memory system. These banks are further subdivided into a number of pages that can range in size from 1 kilobyte (Kbyte) to 64 Kbyte.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 5. Document ID: US 6523092 B1

L27: Entry 5 of 11 File: USPT Feb 18, 2003

DOCUMENT-IDENTIFIER: US 6523092 B1
TITLE: Cache line replacement policy enhancement to avoid memory page thrashing

Detailed Description Text (18):
In a chipset memory controller, memory is typically divided into a number of banks. The particular number of

memory banks deployed in any platform depends on factors such as the DRAM technology used and the number of devices populating the system. With a single dual in-line memory module (DIMM) of synchronous DRAM (SDRAM) for example, a computer system can have as few as four banks. In a fully populated Rambus DRAM (RDRAM) memory subsystem, the chipset can control about a thousand banks. The size of a bank is equal to the size of the memory system divided by the number of banks in the memory system. These banks are further subdivided into a number of pages that can range in size from 1 kilobyte (Kbyte) to 64 Kbyte.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 6092225 A

L27: Entry 6 of 11 File: USPT Jul 18, 2000

DOCUMENT-IDENTIFIER: US 6092225 A
TITLE: Algorithmic pattern generator for integrated circuit tester

Detailed Description Text (23):
FIG. 2 illustrates cache memory system 28 and vector memory 20 of FIG. 1 in more detailed block diagram form. Cache memory system 28 includes a cache controller 36, a set of four main cache memories M1-M4 and one subroutine cache memory C1. Each cache memory occupies a separate portion of a common cache memory address space and each includes a pair of independently addressed cache memory banks A and B. The memory bank A and B of each main cache memory M1-M4 is further subdivided into two independently addressable blocks A1 and A2 or B1 and B2. The A and B banks of subroutine cache C1 include only one block A1 or B1. Each cache memory block A1 or B1 has 256 addressable storage locations, each capable of storing eight vectors. When loading a block of vectors into cache memory, cache controller 36 writes the vectors in alternating fashion into successive addresses of blocks A and B of one of the cache memories. When reading vectors out of a cache memory, cache controller 36 supplies separate read addresses to bank A and bank B causing banks A and B to read out two 8-vector sets VAA-VAH and VBA-VBH, respectively, to vector alignment circuit 30 of FIG. 1. Since banks A and B are independently addressable, cache controller 36 may increment either the A or B bank address in order to advance the vector address sequence.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 7. Document ID: US 6005624 A

L27: Entry 7 of 11 File: USPT Dec 21, 1999

DOCUMENT-IDENTIFIER: US 6005624 A
TITLE: System and method for performing motion compensation using a skewed tile storage format for improved efficiency

Detailed Description Text (27):
In the preferred embodiment of the invention, the motion compensation block 110 includes a memory controller 120 which operates to read reference blocks or prediction blocks from the frame store memory 112. When retrieval of a reference block from the frame store memory 112 requires one or more page crossings, the memory controller 120 reads the entire relevant portion from a respective page before a page crossing or cross miss occurs, i.e., before the memory controller 120 begins reading another reference block portion from another page. In the examples of FIG. 4, the memory controller 120 which performs the read operation is sufficiently intelligent to read or subdivide the prediction macroblock (the shaded area of FIGS. 4a-4c) into three regions, where each one resides on a different page. The memory controller 120 reads each one of these subdivision blocks in turn. Thus the memory

controller 120 reads all of the shaded portion from the first macroblock or first page, then all of the shaded portion from the second macroblock or second page, and then all of the shaded portion from the third macroblock or third page.

☐ 8. Document ID: US 5912676 A

L27: Entry 8 of 11 File: USPT Jun 15, 1999

DOCUMENT-IDENTIFIER: US 5912676 A
TITLE: MPEG decoder frame memory interface which is reconfigurable for different frame store architectures

Detailed Description Text (79):
As described above, when retrieval of reference block data from the frame store memory 204 requires one or more page crossings, the slave device submits a request for each of the pages where the data resides or where the data is to be written. The memory controller 234 operating in response to the programmed memory transfer values reads or writes the entire relevant portion from a respective page before a page crossing or cross miss occurs, i.e., before the memory controller 234 begins reading another reference block portion from another page. For example, if the desired reference block data resides on three pages, the slave device is sufficiently intelligent to program the memory transfer values for three separate transfers. Accordingly, the slave device submits three different requests with three different sets of memory transfer values. In response to these three requests, the memory controller 234 performs the reads or subdivides the prediction macroblock into three regions, where each one resides on a different page. The memory controller 234 reads each one of these subdivision blocks in turn. Thus the memory controller 234 reads all of the shaded portion from the first macroblock or first page, then all of the shaded portion from the second macroblock or second page, and then all of the shaded portion from the third macroblock or third page.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 9. Document ID: US 5453790 A

L27: Entry 9 of 11 File: USPT Sep 26, 1995

DOCUMENT-IDENTIFIER: US 5453790 A
**** See image for Certificate of Correction ****
TITLE: Video decoder having asynchronous operation with respect to a video display

Brief Summary Text (45):
Yet another feature of the present invention is that said units are subdivided in a plurality of categories, units corresponding to different categories carrying different information relating to a same image element, and that said units of video information of different categories are processed by said decoding means regardless of their category said memory module controller demultiplexing said units according to the category they belong to by writing said units in appropriate memory locations within said memory module.

CLAIMS:

6. Video decoder according to claim 4, wherein each of said new units (NEW1), said stored new units (NEW2) and said old units (OLD) is subdivided into a plurality of different parts, each of said different parts of each unit corresponding to different categories (LUM, CHR) of a video image, each of said different parts of each unit

containing video information relating to a same video image, and that said parts of said new units (NEW1) and said old units (OLD) of video information of different categories are processed by said decoding means (DEC1, DEC2) regardless of their category and that said memory module controller (FSC) demultiplexes said parts of said new units (NEW1) and said old units (OLD) according to the category they belong by writing said parts of said new units (NEW1) and said old units (OLD) in appropriate memory locations within said memory module (FSM).

☐ 10. Document ID: US 5305425 A

L27: Entry 10 of 11 File: USPT Apr 19, 1994

DOCUMENT-IDENTIFIER: US 5305425 A
TITLE: Method of and apparatus for evaluating membership functions or rules in fuzzy reasoning system

Detailed Description Text (69):
FIG. 20 is a functional block diagram showing blocks attained by functionally subdividing the system configuration of FIG. 1 into several blocks. A fuzzy reasoning section 31 corresponds to the fuzzy controller 10. A conformity grade keeping section 32 is associated with the memory 22 of the monitor/controller 20 and a similarity computing section 34 and a similarity rule grouping section 35 correspond to the CPU 21. A display section 36 is associated with the display 24.

☐ 11. Document ID: US 4476526 A

L27: Entry 11 of 11 File: USPT Oct 9, 1984

DOCUMENT-IDENTIFIER: US 4476526 A
**** See image for Certificate of Correction ****
TITLE: Cache buffered memory subsystem

Brief Summary Text (24):
The above needs of the art and objects of the invention are satisfied by the present invention which comprises a solid state cache memory unit which comprises random access memory storage devices and a cache memory controller unit. The cache memory unit is operatively connected to disk or other long-term memory storage directors such that several directors can simultaneously direct data to and read data from the cache. The directors in turn are connected by individual channels to host computers. Further, the cache memory of the invention may be connected to disk drives of the dual port type in which plural directors can access a single string of disk drives so that plural tasks can be performed simultaneously on the same string of disk drives. Provision of cache memory space management functions in the cache memory subsystem rather than in the host allows the host to be freed from data storage management (as compared to certain prior art expedients discussed below), while permitting the cache manager to be adaptable for use with differing types of disk drives, in differing system arrangements and permitting of future enhancement. In a preferred embodiment, means are provided for detection of sequential data so that no performance loss is encountered by useless caching of randomly accessed data sets. Similarly, in a preferred embodiment, means are provided for varying the relative size of subdivisions of the cache memory space to match the length of the records most frequently accessed, so as to provide more efficient use of the cache memory area.

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Terms	Documents
L23 same (subdivi$6 or sub-divi$6)	11

Display Format: - Change Format

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